Docket No.: 57454-963 **PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**


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| In re Application of | : | Customer Number: 20277 |
| **Hiroshi Maeda, et al.** | : | Confirmation Number: 5440 |
| Serial No.: 10/633,576 | : | Group Art Unit: 2811 |
| Filed: August 05, 2003 | : | Examiner: To be Assigned |

For: SEMICONDUCTOR DEVICE WITH CAPACITOR ELECTRODES AND METHOD OF MANUFACTURING THEREOF

## SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Mail Stop IDS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This Information Disclosure Statement and 1449 Form is supplemental to that filed August 5, 2003. The reason for this supplemental Information Disclosure Statement and 1449 Form is to correct a typographical error made on the initial 1449 Form.. The last listed Prior Art Publication was initially filed with a typographical error in the title. The title should be changed to read: "Copper Dual **Damascene** Wiring....." as indicated on attached copies.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

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**Date: November 13, 2003**

| INFORMATION DISCLOSURE CITATION IN AN APPLICATION (PTO-1449) | ATTY. DOCKET NO. **57454-963** | SERIAL NO. **Divisional of Serial No. 09/903,735** |
|---|---|---|
| | APPLICANT **Hiroshi MAEDA, ET AL.** | |
| | FILING DATE **August 5, 2003** | GROUP **To be assigned** |



**U.S. PATENT DOCUMENTS**

| EXAMINER'S INITIALS | PATENT NO. | DATE | NAME | CLASS | SUBCLASS | FILING DATE |
|---|---|---|---|---|---|---|
| | 6,424,011 | 07/2002 | Assaderaghi et al | 257 | 350 | |
| | 6,255,151 | 07/2001 | Fukuda et al | 257 | 296 | |
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**FOREIGN PATENT DOCUMENTS**

| EXAMINER'S INITIALS | PATENT NO. | DATE | COUNTRY | CLASS | SUBCLASS | Translation | |
|---|---|---|---|---|---|---|---|
| | | | | | | Yes | No |
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**OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)**

| | |
|---|---|
| | M. Igarashi, A. Harada, H. Amishiro, H. Kawashima, N. Morimoto, Y. Kusumi, T. Saito, A. Ohsaki, T. Mori, T. Fukada, Y. Toyoda, K. Higashitani, and H. Arima, "The Best Combination Of Aluminum and Copper Interconnects For a High Performance 0.18μm CMOS Logic Device," IEDM98, 1998, PP. 829-832. |
| | J. Heidenreich, D. Edelstein, R. Goldblatt, W. Cote, C. Uzoh, N. Lustig, T. McDevitt, A. Stamper, A. Simon, J. Dukovic, R. Wachnik, H. Rathore, S. Luce, and J. Slattery, "Copper Dual **Damascene** Wiring for Sub-0.25μm CMOS Technology," PP. 13-15. |
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| EXAMINER | DATE CONSIDERED |
|---|---|
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.